



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/821,985

04/12/2004

Masayuki Koyama

70456-028

2075

7590 05/30/2008  
McDermott, Will & Emery  
600 13th Street, N.W.  
Washington, DC 20005-3096

EXAMINER

UNELUS, ERNEST

ART UNIT

PAPER NUMBER

2181

MAIL DATE

DELIVERY MODE

05/30/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/821,985	<b>Applicant(s)</b> KOYAMA, MASAYUKI	
	<b>Examiner</b> ERNEST UNELUS	<b>Art Unit</b> 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 May 2008.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-9 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

**DETAILED ACTION**

**RESPONSE TO AMENDMENT**

**Claim rejections based on prior art**

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/05/08 has been entered.

Applicant's arguments filed 05/05/2008, with respect to the rejection(s) of claim(s) 1, 3-8 under Ganapathy et al. (US 2002/0038393) and Levenstein (US 5,586,331) have been fully considered and is not persuasive. However, base on the amendment, the rejection has been withdrawn, and upon further consideration, a new ground(s) of rejection is made in view of Ganapathy et al. (US 2002/0038393).

**This argument is not found to be persuasive;**

**In regards to ‘a group of registers (see fig. 5, which discloses a control register and a channel register inside a DMA; see also paragraph 0029, which discloses “There are DMA descriptor registers in the DMA controllers 203. One or more of these instructions can be written into the DMA descriptor registers while the DMA is in progress and can cause the appropriate action to be performed”) for next transfer which is different from said group of registers for current transfer’ (see paragraph 0019, which discloses a round-robin arbitration scheme on the system bus 200 for the DMA master controllers 203A-203N, 207 and 215, which means, the current DMA is different from the next one),**

### **INFORMATION CONCERNING OATH/DECLARATION**

#### **Oath/Declaration**

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

### **INFORMATION CONCERNING DRAWINGS**

#### **Drawings**

3. The applicant's drawings submitted are acceptable for examination purposes.

### **III. REJECTIONS BASED ON PRIOR ART**

#### **Claim Rejections - 35 USC § 102**

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1 and 3-8**, are rejected under 35 U.S.C. 102(b) as being anticipated by Ganapathy et al. (US 2002/0038393).

6. As per **claim 1**, Ganapathy discloses a direct memory access controller (**system on chip (SOC) 100 of fig. 2, see abstract, which discloses “A distributed direct memory access**

**(DMA) method, apparatus, and system is provided within a system on chip (SOC) ")**

coupled with an arbiter **(bus arbitrators 201A-201N)**, which arbitrates a bus right between the direct memory access controller and another circuit **(network, as discloses in fig. 2)**, comprising:

a plurality of direct memory access transfer portions **(core processors 202A-202N)** controlling direct memory access transfer **(see paragraph 0019, which discloses the DMA master controllers 203A-203N, 207, and 215, which are inside the core processors, gaining access on system bus 200);** and

a control portion **(bus master 203A-203N, see fig. 2 and paragraph 0019)** permitting use of a bus by said plurality of direct memory access transfer portions **(see paragraph 0019, which discloses “A round-robin arbitration scheme on the system bus 200 assures that each of the distributed DMA master controllers 203A-203N, 207 and 215 have access every so often to the system bus 200 and can access the global memory 210 at that time” at a predetermine interval, using the round scheme, each of the master controller 203A-203N, which is inside of a core processor, which has channel, as indicated in paragraph 0026, has access or ownership to the bus)**, in response to transfer requests from said plurality of direct memory access transfer portions **(paragraph 0020 discloses transfer requests from the said plurality of direct memory access transfer portions, 202A-200N)**, while the bus ownership is granted to the direct memory access controller from said arbiter **(see also paragraph 0019, which discloses “Access to the central system bus 200 by function modules of the system on a chip 100 is arbitrated by bus arbitrators 201A-201N coupled to the system bus 200 using a uniform programmable arbitration protocol”;** and

two groups of registers (**the descriptor registers in the DMA controllers 203 for a current transfer controller and the descriptor registers of the next controller. see fig. 5, which discloses a control register and a channel register inside a DMA; see also paragraph 0029, which discloses “There are DMA descriptor registers in the DMA controllers 203. One or more of these instructions can be written into the DMA descriptor registers while the DMA is in progress and can cause the appropriate action to be performed”**) including a first group for current transfer and a second for next transfer which is different from said first group for current transfer (**see paragraph 0019, which discloses a round-robin arbitration scheme on the system bus 200 for the DMA master controllers 203A-203N, 207 and 215, which means, the current DMA is different from the next one**), values (addresses) set in two groups being for controlling the direct memory access transfer (**see paragraph 0020, which discloses “A register is set up during a DMA that allows addresses to be automatically generated and multiple data blocks or bytes to be accessed in sequence”**). See fig. 5 and paragraph 0029 for further detail. Since this is a round robin scheme, the next DMA transfer will be in a current state, once it gains ownership of the bus),

wherein said control portion permits transferring to a first portion of said direct memory access transfer portions based on values set in said first group (**see fig. 3, which also discloses data going from the bus to the core processors, see paragraph 0043 for further detail**), and permits transferring to a second portion of said direct memory access transfer portions based on values set in said second group after transferring by said first portion, in one granting period of transferring by the arbiter (**see paragraph 0019, which discloses the round-robin arbitration scheme**).

7. As per **claim 3**, Ganapathy discloses “the direct memory access controller according to claim 1” [See rejection to **claim 1** above], wherein to said second group for next transfer (**the registers in the DMA controllers 207 of fig. 5, as also discloses in paragraph 0029**), direct memory access control information stored in an external memory is successively transferred and stored (**paragraph 0021**).

8. As per **claim 4**, Ganapathy discloses, wherein transfer of the direct memory access control information from said external memory to said second group for next transfer is performed after previous values stored in said second group for next transfer to said first group for current transfer are transferred and before bus ownership is switched among said plurality of direct memory access transfer portions (**paragraph 0025 discloses “In any case, the data that needs processing is stored into the global buffer memory 210 first. The one or more core processors 202A-202N then retrieve the data for the given channel for processing”**).

9. As per **claim 5**, Ganapathy wherein said control portion determines order of bus use by said plurality of direct memory access transfer portions in accordance with round robin method (**paragraph 0019 discloses “A round-robin arbitration scheme on the system bus 200 assures that each of the distributed DMA master controllers 203A-203N, 207 and 215 have access every so often to the system bus 200 and can access the global memory 210 at that time”**).

10. As per **claim 6**, Ganapathy discloses, wherein said control portion determines order of bus use by said plurality of direct memory access transfer portions in accordance with past

number of direct memory access transfers by each channel (**paragraph 0037 discloses “the data is time division multiplexed on the serial data stream into time slots for each communication channel. Because the distributed DMA of the present invention is particularly suited to support blocks of data for given channels, the serial port provides interleaving and deinterleaving of data from the serial data stream for each channel”**).

11. As per **claim 7**, the combination of Ganapathy and Levenstein discloses “the direct memory access controller according to claim 1” [See rejection to claim 1 above], Ganapathy further discloses, wherein in said control portion (**bus arbitrators 201A-201N**), number of transfers made by each channel while one continuous bus ownership is being granted is set (**see paragraph 0038**), and said control portion permits use of the bus among said plurality of direct memory access transfer portions in accordance with said number of transfers (**paragraph 0038, this is done using the round-robin**).

12. As per **claim 8**, Ganapathy discloses, wherein in said control portion (**bus arbitrators 201A-201N**), an order of bus (**round-robin**) use by channels is set when there are three or more channels (**Ganapathy discloses multiply channels, for example, connections between the bus master (203A-203N) to the system bus (200), see fig. 2**), and bus (**200**) use is permitted among said plurality of direct memory access transfer portions (**core processors 202A-202N**) in accordance with the order (**round-robin**) of bus use (**paragraph 0019**).



**Claim Rejections - 35 USC § 103**

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

14. **Claim 9**, is rejected under 35 U.S.C. 103(a) as being unpatentable over Ganapathy et al. (US 2002/0038393) in view of Levenstein (US 5,586,331).

15. As per **claim 9**, Ganapathy discloses “the direct memory access controller according to claim 1” [See rejection to claim 1 above], but fails to further disclose expressly comprising a cycle steal control circuit, wherein said control portion permits said first and second portions of said direct memory access transfer portions by a cycle steal manner controlled by said cycle steal control circuit.

Levenstein discloses a cycle steal control circuit, wherein said control portion permits said first and second portions of said direct memory access transfer portions by a cycle steal manner controlled by said cycle steal control circuit (see col. 6, lines 41-46, which also discloses “Register 146 also is used in providing information as to the need to purge a line in the cache memory, and to generate a cycle "steal" for this purpose”. See col. 8, lines 36-44 for further detail).

Ganapathy et al. (US 2002/0038393) and Levenstein (US 5,586,331) are analogous art because they are from the same field of endeavor of arbitrating multiple processors.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a distributed direct memory access (DMA) method, apparatus, and system is provided within a system on chip (SOC) as described by Ganapathy and an information processing systems in which multiple processing devices are coupled to a main storage memory or other shared resource, and more particularly to means for allocating access to the shared resource among the processing devices as taught by Levenstein.\

The motivation for doing so would have been because Levenstein teaches, **“As compared to conventional networks, a data processing network according to the present invention is thus more compact and requires less "bureaucracy", for substantially improved performance”** (see col. 2, lines 38-41).

Therefore, it would have been obvious to combine Levenstein (US 5,586,331) with Ganapathy et al. (US 2002/0038393) for the benefit of creating the direct memory access controller to obtain the invention as specified in claim 9.

#### **RELEVANT ART CITED BY THE EXAMINER**

16. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

17. The following reference teaches a direct memory access controller comprising a plurality of direct memory access transfer portions.

**U.S. PATENT NUMBER**

US 5,794,070

**CLOSING COMMENTS**

**Conclusion**

**a. STATUS OF CLAIMS IN THE APPLICATION**

18. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

**a(1) CLAIMS REJECTED IN THE APPLICATION**

19. Per the instant office action, claims 1 and 3-9 have received a first action on the merits and are subject of a first action non-final.

**DIRECTION OF FUTURE CORRESPONDENCES**

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

**IMPORTANT NOTE**

21. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Alford Kindred, can be reached at the following telephone number: Area Code (571) 272-4037.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or

Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PMR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217- 91 97 (toll-free).

May 27, 2008

Ernest Unelus  
Patent Examiner  
Art Unit 2181

/E. U./

Examiner, Art Unit 2181

/Alford W. Kindred/  
Supervisory Patent Examiner, Art Unit 2163